WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a plurality of unit memory cells, wherein a unit memory cell comprises:

a first planar transistor in a semiconductor substrate; and

a vertical transistor disposed on the first planar transistor;

a second planar transistor in the semiconductor substrate in series with the first planar transistor.

2. The semiconductor memory device of Claim 1, wherein the semiconductor memory device further comprises a plurality of word lines.

3. The semiconductor memory device of Claim 2, wherein one of the word lines comprises a gate of the second planar transistor.

4. The semiconductor memory device of Claim 1, wherein the first planar transistor includes a storage node, and wherein the storage node comprises the gate of the first planar transistor.

5. The semiconductor memory device of Claim 4, wherein the storage node further comprises the source of the vertical transistor.

6. The semiconductor memory device of Claim 4, wherein the first planar transistor further comprises a first conductive region and a second conductive region.

7. The semiconductor memory device of Claim 6, wherein the first planar transistor further comprises a channel region disposed between

the first conductive region and the second conductive region, and wherein the storage node is disposed only on a first portion of the channel region.

8. The semiconductor memory device of Claim 7, wherein a portion of the first conductive region adjacent the channel is lightly doped as compared to a portion of the second conductive region adjacent the channel.

9. The semiconductor memory device of Claim 8, wherein the vertical transistor further comprises a multi-junction storage pattern on the storage node, a data line on the multi-junction storage pattern, and a word line that is on the data line.

10. The semiconductor memory device of Claim 9, wherein the word line is also on the second channel region.

11. The semiconductor memory device of Claim 9, further comprising a capping insulation pattern between the data line and the word line.

12. The semiconductor memory device of Claim 1, wherein the first planar transistor and the second planar transistor have different threshold voltages.

13. A unit cell of a semiconductor memory device, comprising:

a substrate having a first conductive region and a second conductive region separated by a channel region;

a storage node disposed solely on a first portion of the channel region;

a multi-tunnel junction pattern on the storage node;

a data line on the multi-tunnel junction pattern; and

a word line on the data line, on sidewalls of the multi-tunnel junction pattern and the storage node and on a second portion of the channel region.

14. The unit cell of Claim 13, further comprising a gate insulation pattern between the storage node and the semiconductor substrate.

15. The unit cell of Claim 13, wherein a portion of the first conductive region adjacent the channel is only lightly doped while a portion of the second conductive region adjacent the channel is heavily doped.

16. The unit cell of Claim 13, further comprising a capping insulation pattern between the data line and the word line.

17. The unit cell of Claim 13, wherein the first and second conductive regions, the channel region and the storage node comprise a first transistor.

18. The unit cell of Claim 17, wherein the storage node, the multi-junction pattern, the data line and the word line comprise a second transistor that is disposed in a perpendicular orientation with respect to the first transistor.

19. The unit cell of Claim 18, wherein the word line and the second portion of the channel region comprise a third transistor.

20. The unit cell of Claim 19, wherein the first transistor and the third transistor have different threshold voltages.

21. The unit cell of Claim 13, wherein the first portion of the channel region and the second portion of the channel region have different doping concentrations.

22. A method of manufacturing a semiconductor memory device, the method comprising:

sequentially forming a storage node and a multi-tunnel junction pattern on a first portion of a channel region defined in a semiconductor substrate to form a stacked multi-layered pattern on the first portion of the channel region;

forming a data line on the multi-layered pattern;

forming a first conductive region adjacent the multi-layer pattern and forming a second conductive region adjacent a second portion of the channel region;

forming a gate interlayer insulating layer on the data line; and

forming a word line on the gate interlayer insulating layer and on the second portion of the channel region.

23. The method of Claim 22, further comprising forming a capping insulation layer on the data line prior to forming the word line.

24. The method of Claim 22, further comprising forming a gate insulation pattern on the first portion of the channel region prior to forming the storage node.

25. The method of Claim 22, wherein forming the first conductive region adjacent the multi-layer pattern and forming the second conductive region adjacent the second portion of the channel region comprises:

forming a mask pattern defining the second portion of the channel region;

forming the first conductive region and the second conductive region in the semiconductor substrate using the mask pattern and the multi-layered pattern as an ion implantation mask; and

removing the mask pattern.

26. The method of Claim 25, further comprising performing an ion implantation process for adjusting a threshold voltage prior to forming the mask pattern.

27. The method of Claim 22, wherein forming the first conductive region adjacent the multi-layer pattern and forming the second conductive region adjacent the second portion of the channel region comprises:

forming a first mask pattern over at least the second channel region;

forming a first lightly doped region and a second lightly doped region in the semiconductor substrate via ion implantation using the first mask pattern and the multi-layered pattern as an ion implantation mask;

removing the first mask pattern;

forming a spacer on the sidewalls of the multi-layered pattern;

forming a second mask pattern over at least the second channel region;

forming a first heavily doped region and a second heavily doped region in the semiconductor substrate via ion implantation using the second mask pattern, the multi-layered pattern and the spacer as an ion implantation mask; and

removing the second mask pattern.

28. The method of Claim 22, further comprising forming an upper conductive pattern between the multi-layered pattern and the data line.

29. A method of manufacturing a semiconductor memory device, comprising:

forming a first planar transistor and a second planar transistor in a semiconductor substrate; and

forming a vertical transistor on the first planar transistor;

wherein the second planar transistor is in series with the first planar transistor and wherein a word line of the semiconductor memory device comprises the gate of the second planar transistor.

30. The method of Claim 29, wherein forming a first planar transistor in a semiconductor substrate comprises forming a first conductive region and a second conductive region in the semiconductor substrate to define a channel region therebetween and forming a storage node that comprises the gate of the first planar transistor on only a portion of the channel region.

31. The method of Claim 30, wherein the storage node further comprises the source or the drain of the vertical transistor.

32. The method of Claim 31, wherein forming a first conductive region and a second conductive region in the semiconductor substrate to define a channel region therebetween comprises forming a lightly doped conductive region adjacent one side of the channel and forming a heavily doped conductive region adjacent the other side of the channel.

33. A semiconductor memory device, comprising:

a first planar transistor comprising a storage node, a first conductive region and a second conductive region in a semiconductor substrate, wherein the first conductive region and the second conductive region define a channel region therebetween, and wherein the storage node is only on a first portion of the channel region;

a vertical transistor comprising the storage node, a multi-tunnel junction pattern stacked on the storage node, a data line stacked on the multi-tunnel junction pattern, and a word line that is on the data line and

on sidewalls of the storage node and the multi-tunnel junction pattern; and

a second planar transistor comprising the first and second conductive regions and a portion of the word line that is on a second portion of the channel region.

34. The semiconductor memory device of Claim 33, further comprising a gate insulating pattern between the storage node and the first portion of the channel region.

35. The semiconductor memory device of Claim 33, wherein a first threshold voltage associated with the first planar transistor is different than a second threshold voltage associated with the second planar transistor.

36. The semiconductor memory device of Claim 33, further comprising a gate interlayer insulator between the word line and sidewalls of the storage node, between the word line and sidewalls of the multi-tunnel junction pattern and between the word line and the second portion of the channel region.

37. The semiconductor memory device of Claim 33, further comprising a capping insulation pattern between the data line and the word line.

38. A semiconductor memory device, comprising:

a source region and a drain region in a semiconductor substrate;

a gate that is laterally offset from at least one of the source region and the drain region and provided on the substrate between the source

region and the drain region;

a vertical transistor on the gate.

39. The semiconductor memory device of Claim 38, wherein the gate comprises a storage node.

40. The semiconductor memory device of Claim 39, wherein the storage node comprises a source/drain region of the vertical transistor.

41. A method of manufacturing a semiconductor memory device, comprising:

forming a source region and a drain region of a first planar transistor in a semiconductor substrate;

forming a gate of the first planar transistor on the semiconductor substrate;

forming a vertical transistor on the gate of the first planar transistor such that the gate of the first planar transistor defines a first channel region beneath the gate of the first planar transistor and a second channel region outside the gate of the first planar transistor;

forming a word line on the second channel region.

42. The method of Claim 41, wherein the gate of the first planar transistor is on only a portion of the channel region.

43. The method of Claim 42, wherein the gate of the first planar transistor further comprises the source or the drain of the vertical transistor.

44. The method of Claim 41, further comprising forming a second planar transistor at the second channel region.